METHOD AND APPARATUS FOR ADDRESS DECODING OF EMBEDDED DRAM DEVICES

ABSTRACT

A method for decoding a memory array address for an embedded DRAM (eDRAM) device is disclosed, the eDRAM device being configured for operation with an SDRAM memory manager. In an exemplary embodiment of the invention, the method includes receiving a set of row address bits from the memory manager at a first time. A set of initial column address bits is then subsequently from the memory manager at a later time. The set of initial column address bits are translated to a set of translated column address bits, and the set of row address bits and the set of translated column address bits are simultaneously used to access a desired memory location in the eDRAM device. The desired memory location in the eDRAM device has a row address corresponding to the value of the set of row address bits and a column address corresponding to the value of the set of translated column address bits.